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SOLID-STATE WIDE-RANGE LOW POWER CAMERA TIMER FOR SPACE APPLICATIONS

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BY

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By

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INTRODUCTION

Rocket-borne camera instruments require some type of timing control device to open and close a camera shutter several times during a rocket flight. The camera shutter is opened for a preset period of time for a given exposure and then closed for a sufficient time to advance the film to the next frame before it is opened again. The timer described in this paper was developed to control the shutter of a camera designed to take preset time exposures of the sun during the flight of an Aerobee Rocket. The film exposure times required varied from a fraction of a second to several hundred seconds with a tolerance of plus or minus 10% from the nominal values. The tolerance required was no more stringent than this because the actual flight exposure time was telemetered back to the ground for use in analysing the photographs.

Timing devices usually employed use either a fixed-frequency-oscillator clock driving a chain of flip-flop scalers

or a variable-frequency-oscillator clock driving a chain of flip-flop scalers with a diode matrix on the scalers to control the frequency of the clock. Both of these systems use a relatively high-frequency basic-oscillator clock to determine the minimum timing interval, and a long sequence of flip-flop scalers to obtain a long timing interval. These timing devices have functioned quite satisfactorily on rockets in the past but they have had the disadvantage of not being very flexible. In the first case a large number of gates are connected in a specific way to obtain a given timing sequence and timing interval, and it is difficult to change these gates after the timer is fabricated; in the second case there is a limit to the dynamic range of the single variable-frequency oscillator and this controls the maximum time that can be obtained for a given minimum time.

Many of the circuits used in the timer described in this paper were developed by the Experimental Systems Section of the Solar Physics Branch of the Goddard Space Flight Center for satellite payloads. These circuits require very low average power and have proven quite reliable in satellite instruments.

POWER SUPPLY AND SIGNAL ISOLATION

The camera and low-level electronic circuits for this experiment were mounted in a package atop the rocket in an attitude controlled "pointed section". This experiment pointed section has a somewhat limited space and weight allowance; therefore, the camera shutter timer and experiment battery

supply were mounted in a pressurized compartment below the pointed section. This separation introduced an unavoidable ground loop, because the pointed section battery common was connected to the chassis at two points; near the low-level amplifiers in the pointed section and at the data-handling system battery supply common in a lower rocket compartment. This ground loop was one source of noise. There were other noise pulse sources caused by pulse currents flowing during the operation of the shutter and film transport solenoids, the pointed section torque motor, relays, timing circuits controlling various rocket functions and the data handling telemetry transmitter.

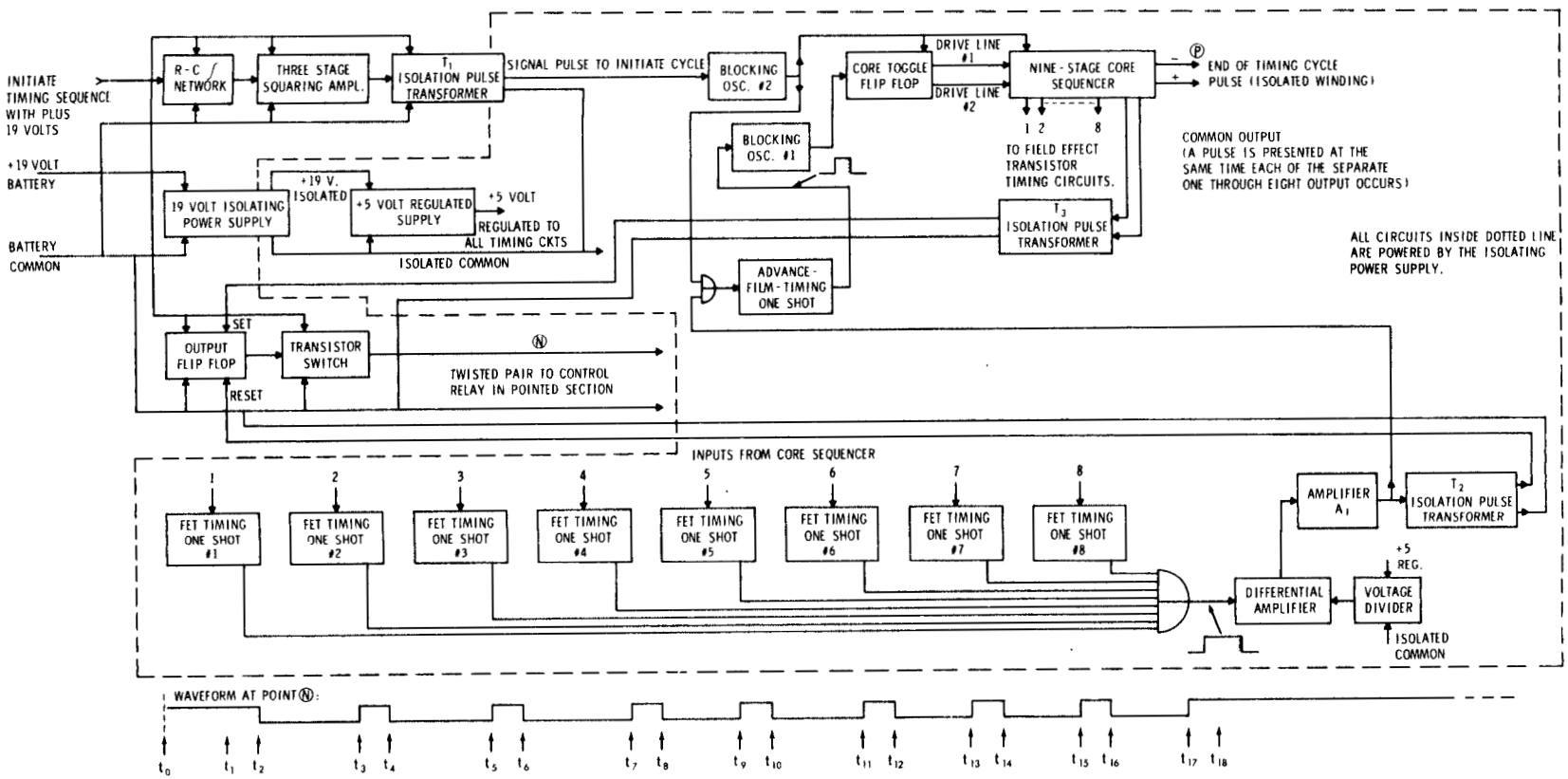
In order to reduce the coupling of these noise signals into the timer, all of the timing and sequencing circuits were powered from an isolating dc-to-dc converter power supply and in addition, all signal pulses interfacing with the experiment battery and the isolating power supply were coupled through special pulse transformers. These pulse transformers were segment wound to reduce the primary-to-secondary capacitance to a minimum and thus eliminate spurious capacitively-coupled pulses from triggering the timing control circuits.

A test was made on a complete breadboard circuit to determine the effectiveness of the aforementioned isolation techniques. A noise pulse current was applied by a pulse

generator in series with the battery supply common lead. This pulse was 10 microseconds long with a fraction of a microsecond rise time. The maximum peak pulse amplitude available from the signal generator was 5 amperes. This magnitude of current, of either polarity, did not spuriously trigger the timer. The timer did trigger spuriously with the same negative-going pulse at a magnitude of approximately 200 milliamperes when the battery and isolation power supply common leads were connected together. This is a good indication of the effectiveness of the isolation techniques.

BLOCK DIAGRAM

Figure 1 is a simplified block diagram of the complete timer, including a waveform diagram showing the voltage signal produced on the output transistor. Electronic circuits in the pointed section were designed to recognize each positive-going transition in this waveform, i.e. t_3, t_5,etc., and to command the film transport mechanism to step the film one position at each transition. These time intervals, t_3 to t_4, t_5 to t_6, etc., were all of equal length and were adjusted to be somewhat longer than the time required to move the film one position. The camera shutter was opened by circuits in the pointed section during the time intervals t_2 to t_3, t_4 to t_5, etc., and the camera shutter was closed during all of the other intervals. There are 8 of these timing intervals in this timer with the time period of each interval controlled by a separate one-shot timer. The separate one-shot timers make it possible to



t_0 : POWER ON

t_1 : INITIATE TIMING CYCLE - BEGIN ADVANCE FILM ONE SHOT TIME - PRESET CORE SEQUENCER AND CORE FLIP FLOP.

t_2 : END OF ADVANCE FILM ONE SHOT TIME AND BEGINNING OF 1ST EXPOSURE TIMING INTERVAL.

t_3 : END OF 1ST EXPOSURE AND BEGINNING OF 1ST ADVANCE FILM ONE SHOT TIMING INTERVAL.

t_4 : END OF 1ST ADVANCE FILM INTERVAL AND BEGINNING OF 2ND EXPOSURE TIMING INTERVAL.

t_5 : THRU t_{17} REPEATS THE ABOVE CYCLE TO CARRY THE SEQUENCE THRU 8 EXPOSURE TIMING INTERVALS AND 7 FILM ADVANCE INTERVALS.

t_{18} : END OF THE 9TH AND LAST ADVANCE FILM TIMING INTERVAL ONE SHOT. A PULSE APPEARS AT POINT Ⓟ ABOVE AT THIS TIME.

Figure 1. Rocket Experiment Timer for Camera Shutter And Film Advance Control

independently control each exposure time interval and, in the actual unit, timing resistors and capacitors were made accessible so that timing changes could be made right up to the time of flight.

The output flip-flop shown in Figure 1 is arranged to have a preferred state, when the power is applied to the timer at time t_o, to assure that the output transistor switch remains off at power turn-on. The timing cycle is initiated, after a minimum time delay of approximately 6 seconds from power turn-on, by applying a voltage to the input of the 3-stage squaring amplifier (a minimum time delay is necessary, as will be explained later, because of the manner in which the field effect transistor (FET) timer one-shots perform at power turn on). When this voltage is applied, a pulse appears on the secondary winding of the isolating pulse transformer, T1. This voltage pluse triggers single-shot blocking oscillator number 2, which presets the core toggle flip flop and the core sequencer and triggers the advance-film-timing one shot. One-shot blocking oscillator number 1 triggers at the end of the advance film timing one-shot interval and drives the core toggle flip-flop which produces an output pulse on output drive line number 1. This output drives a shift line of the core sequencer and a voltage pulse appears at core sequencer output number 1 which triggers FET timing one-shot number 1 and starts the first camera shutter timing interval.

A voltage pulse is also generated at this time on the secondary of isolation transformer, T_3, which triggers the output flip-flop and turns on the output transistor switch (time t_2 in Figure 1).

One side of all of the FET one-shot timing circuits is applied to the input of an "or" gate connected to one input of a differential amplifier (the reason for the differential amplifier will be explained later). At the end of timing interval number 1 a voltage pulse appears at the output of amplifier, A_1, which triggers the advance-film-timing one-shot and, through isolating transformer, T_2, resets the output flip-flop to turn off the output transistor switch to end the first timing interval (time t_3). At the end of the advance film timing one-shot interval blocking oscillator number 1 triggers and the cycle continues as output number 2 of the core sequencer produces a pulse which triggers FET timing circuit number 2. This cycle repeats with each successive trigger of a FET timing one-shot until the end of the last timing interval (time t_{17}).

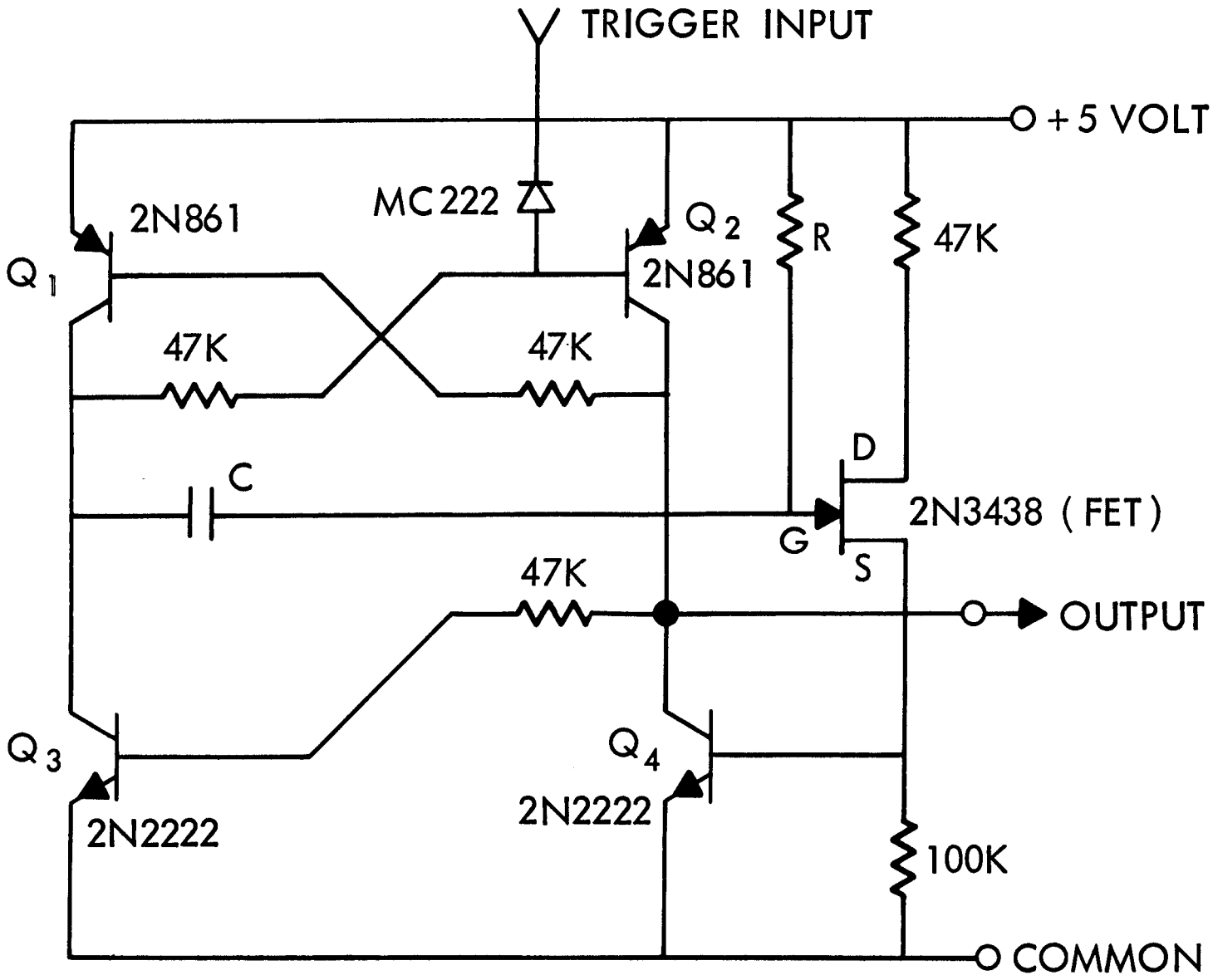
At time, t_{17}, the advance-film-timing one-shot triggers and the output flip flop resets for the last time. At the end of the last advance-film-timing one-shot interval a final pulse is applied to the core sequencer and a pulse appears at point P (time t_{18}), however, the output flip-flop is not set at this time since no pulse appears on the secondary of isolating pulse transformer, t_3. Furthermore, no core in the core sequencer remains preset (binary "one" state) at the completion of the

cycle and any subsequent triggering of the advance-film-timing one shot will not product a pulse on any of the core sequencer outputs to start the cycle at the wrong time. More will be said about this in a later section.

FIELD EFFECT TRANSISTOR TIMING ONE-SHOT CIRCUIT.

Figure 2 shows a circuit of the FET timing-one-shot circuit used in this timer. It is a complimentary-symmetry one-shot with a field effect transistor (FET) in the timing network. The FET has a high input resistance and therefore a relatively large value timing resistance may be used to obtain a much longer delay time than is possible with this circuit without the FET. The FET isolates the timing RC elements from transistor Q_4 and provides gain between the junction of R and C and the base of transistor Q_4.

There were two undesirable features in the operation of the FET-timing-one-shot circuit which had to be taken into account when using it in a practical circuit: the voltage waveform at the trailing edge of the timing interval was not ideal for R-C differentiating and, depending on the length of the timing interval, some time was required for the circuit to reach a quiescent state after the power was applied. The quiescent state is here defined as, the state in which transistors Q_4 and Q_1 have turned on, transistors Q_2 and Q_3 have turned off and capacitor, C, has charged to its maximum voltage (See Figure 2). The voltage waveform at the trailing edge of the timing interval



NOTE: ALL RESISTORS ARE METAL FILM.

Figure 2. Field Effect Transistor

One Shot Circuit

is here defined as the voltage transition from approximately plus 5 volts to zero volts which appears at the output, shown in Figure 2, when transistors Q_1 and Q_4 turn on.

Figure 3 is a drawing of a typical voltage waveform at the trailing edge of a timing interval. A circuit must be made to respond to this waveform to define the timing interval and to trigger other circuits to continue the timer output voltage waveform. It can be seen from Figure 3 that straightforward amplification and squaring of the trailing edge is not a good solution because the time interval t_1 to t_2 would require considerable gain to achieve a fast-rising-voltage trigger pulse. Such high gain at this point should be avoided due to the possibility of noise pulses being amplified and causing spurious triggering. A differential amplifier was used to solve this problem. One input of the amplifier was connected through and "or" gate to the outputs of all 8 FET-timing-one-shot circuits and the other input was connected to a voltage divider. The voltage divider was adjusted so that the differential amplifier changed state at a voltage, v_t, during the maximum time-rate-of-change of the voltage transition. Some voltage gain was introduced following the differential amplifier to obtain a fast-rising pulse for triggering the advance-film-timing one-shot and the output flip-flop.

If a trigger pulse is derived at the output of the differential amplifier each time a negative-going voltage

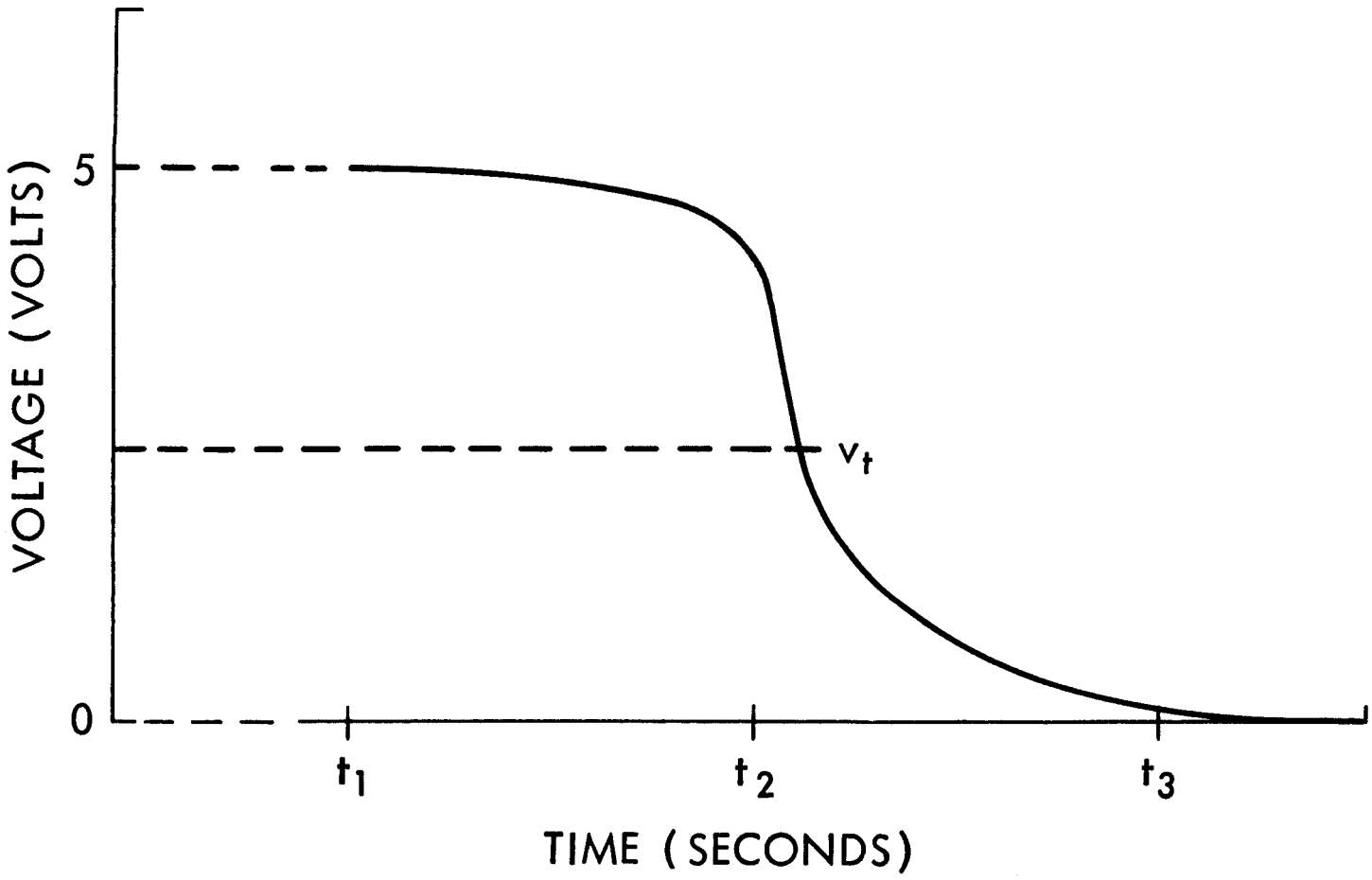


Figure 3.

WAVEFORM OF THE TRAILING EDGE OF THE VOLTAGE TRANSIENT ON THE OUTPUT OF THE FIELD EFFECT TRANSISTOR ONE SHOT CIRCUIT

Time: t_1 to t_2, 6 seconds typical

t_2 to t_3, 150 microseconds typical

transition appears on the output of a FET-timing one-shot, then some protection must be provided to prevent a spurious timing cycle initiation when the FET-timing one-shot goes to its quiescent state some time after power turn on (this time is approximately 6 seconds in a 100 second timing interval). Since voltage pulses from the core sequencer trigger the FET-timing-one-shot circuits to continue the timing cycle the required protection is obtained by arranging the circuit so that it is impossible to obtain a pulse from the core sequencer until the timing cycle is initiated by the application of a voltage to the "initiate timing cycle" input. This will be explained in the section of this paper describing the core sequencer.

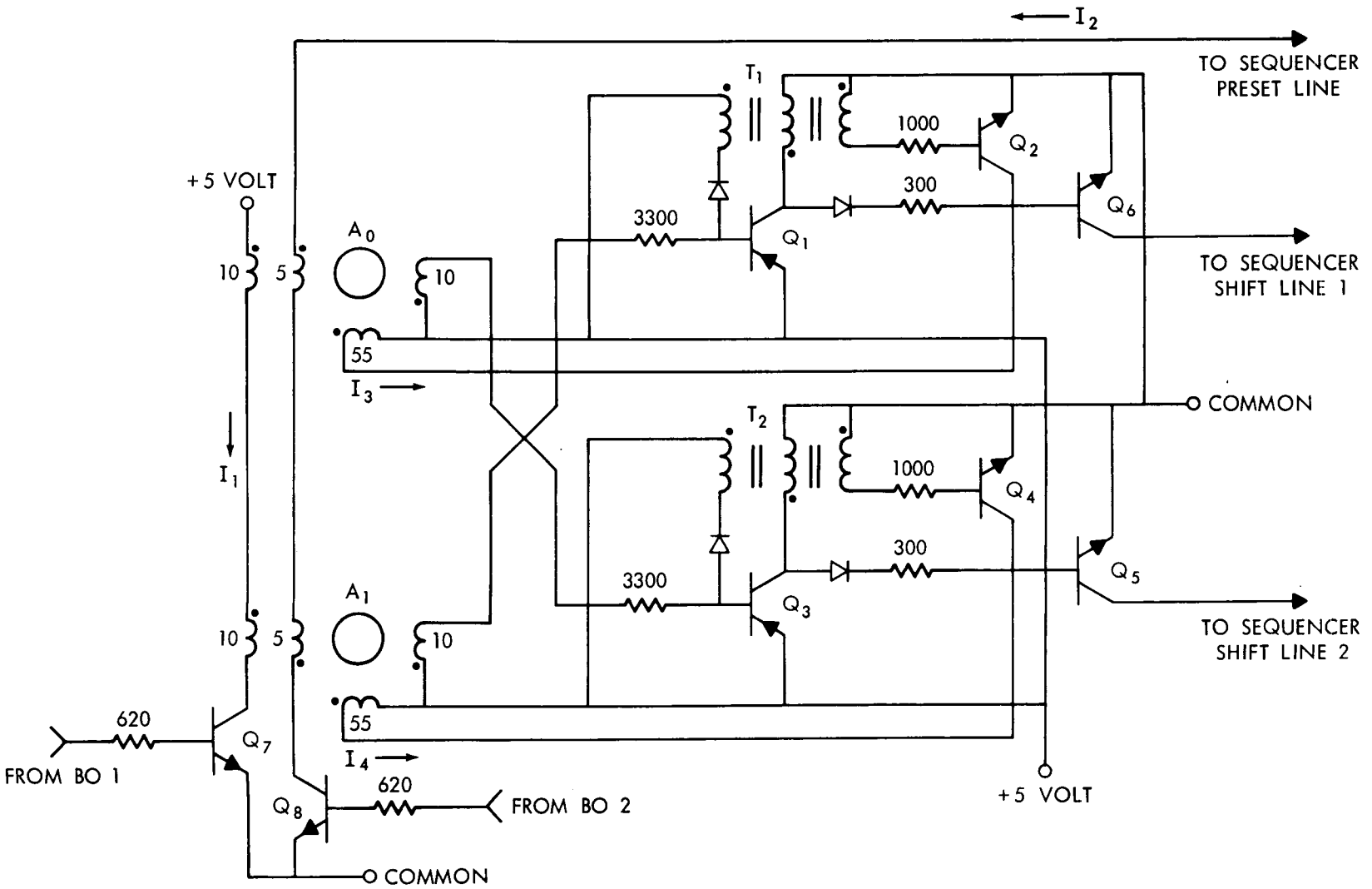
The FET-timing-one-shot circuit has one additional feature which controls the way the timer performs at power turn off and turn on. There is no problem in the normal operation of the timer since the power will remain turned on until the end of the complete timing cycle. A charge will remain on capacitor, C, when the power is removed, which will discharge at a rate determined by the RC-time constant of the circuit. If the power is reapplied before sufficient time has elapsed to completely discharge capacitor, C, the output of the FET-timing-one-shot circuit will be positive and remains positive until the charge has been removed and transistor Q_4 turns on. This means that a proper timing cycle cannot be initiated until a minimum time of the longest FET-timing-one-shot circuit interval is allowed

to elapse between power turn-off and the initiation of a new cycle. In other words if the longest timing interval is 100 seconds then a minimum time of 100 seconds should be allowed to elapse between the time the power is turned off and a new timing cycle is initiated, regardless of when the power is reapplied during the intervening interval.

CORE FLIP FLOP CIRCUIT

Figure 4 is a schematic diagram of the core flip flop. This circuit requires extremely small average power at the low duty cycle rates of this timer. The purpose of this circuit is to provide pulses alternately on sequencer shift line number 1 and number 2 from each pair of pulses applied to the input from BO number 1. The circuit is also arranged so that a pulse occurs on sequencer shift line number 1 when the first BO 1 input pulse is applied.

The core flip flop operates in the following way: first the BO 2 pulse drives transistor switch Q_8 "on" and causes a pulse current, I_2, to flow from the sequencer through a winding on non-linear core transformers A and A . This pulse switches the core of transformer A_0 to the "zero" state and the core of transformer A_1 to the "one" state. Next a BO 1 pulse drives transistor switch Q_7 "on" which causes a pulse current, I_1, to flow from plus five volts through a winding on each of the non-linear core transformers, A_0 and A_1. This pulse switches



NOTE : ALL NON-LINEAR CORES ARE TAPE WOUND 22 MAXWELL 1/8th MIL MO-PERMALLOY.
ALL LINEAR CORES ARE TAPE WOUND 22 MAXWELL 1 MIL MO-PERMALLOY.
NPN TRANSISTORS ARE 2N2222, PNP TRANSISTORS ARE 2N861, DIODES ARE MC222.
ALL WINDINGS ARE # 40 AWG WIRE.

Figure 4. Core Flip-Flop Circuit

the non-linear core of transformer A_1 to the "zero" state, producing a voltage pulse that triggers blocking oscillator transistor Q_1, which in turn drives transistor switch Q_6 "on" and returns sequencer shift line number 1 to power supply common. The width of the pulse that drives transistor switch Q_7 is arranged to be less than the width of the pulse obtained from blocking oscillator transformer T_1. After current pulse, I_1, has returned to zero, the overshoot voltage obtained from blocking oscillator transformer T_1, drives transistor switch Q_2 "On" to produce a pulse current, I_3, which switches the non-linear core of transformer A_o to the "one" state. The next BO 1 pulse drive to transistor switch Q_7 causes the non-linear core of transformer A_o to switch to the "zero" state, producing a voltage pulse that triggers blocking oscillator transistor Q_3, which in turn drives transistor switch Q_5 "on" and returns sequencer shift line number 2 to the power supply common. The overshoot voltage from blocking oscillator transformer T_2 drives transistor switch Q_4 "on" and switches the non-linear core of transformer A_1 to the "one" state. This cycle is repeated for each pair of BO 1 pulses which alternately switches sequencer shift lines 1 and 2, thus providing the desired two-phase signal to the sequencer.

CORE SEQUENCER

A detailed schematic diagram of the core sequencer is shown in Figure 5. The core sequencer provides the following

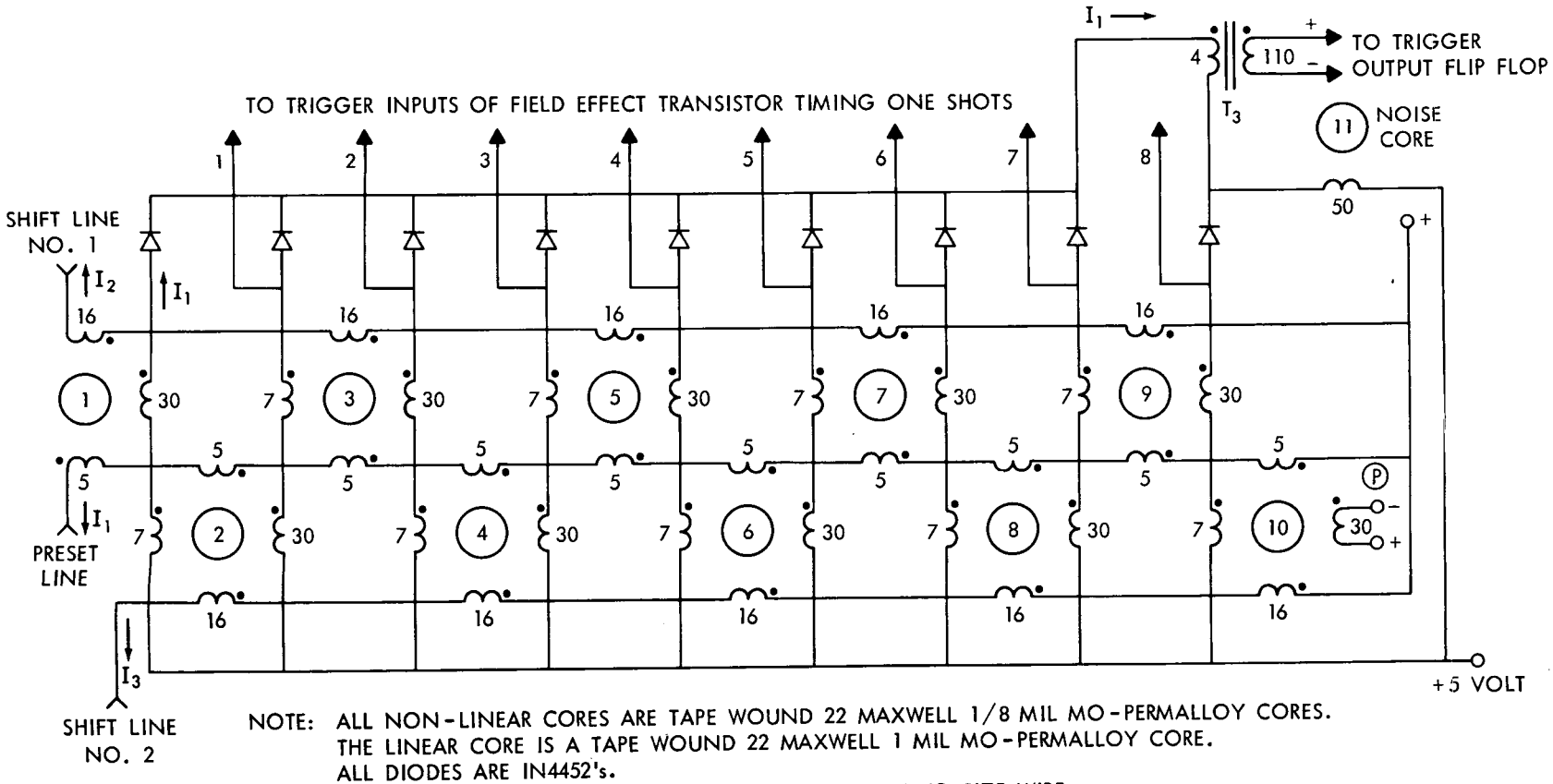


Figure 5. Core Sequencer Circuit

signals: time sequential pulses on 8 separate output lines to trigger the 8 FET one shots; time sequential pulses on one isolated line pair output to trigger the output flip flop; and a single pulse that appears only once on another isolated line pair output at the end of the complete timing cycle. This last pulse was not used in the final version of the timer but it was thought at one time that it would be necessary, therefore, the additional core was connected into the core sequencer when it was fabricated. The core sequencer provides the added feature of allowing no output pulses to appear before the start of an actual timing cycle, even though spurious input signals may occur at power turn on. The reason for this requirement was discussed in a previous section of this paper.

There are 3 series-connected input lines on the core sequencer; a preset line connecting all of the cores in series with 5 turns on each core; one shift line connecting all of the odd-numbered cores in series with 16 turns on each core and another shift line connecting all of the even-numbered cores in series with 16 turns on each core. A current pulse on the preset line switches core number 1 to the "one" state and all of the other cores in this line to the "zero" state. A current pulse on either shift line switches all of the cores on that line to the "zero" state.

The core sequencer will not operate until a pulse is applied to the preset line input. This pulse current, I_1 in Figure 5, switches core number 1 to the "one" state and switches

any other core in the sequencer that may have been in "one" state to the "zero"state. This same current also switches the core of transformer A_1 in the core flip flop to the "one" state. The current pulse magnitude in this line is adjusted so that any core that switches will do so over a relatively long period of time (20 microseconds) and, as a result, the voltage appearing on the output windings will be very small. This prevents the possibility of a trigger pulse appearing at this time on one of the sequencer output lines. In the normal operation of the timer the only cores that will switch at this time are cores number 1 and 10 and the polarity of pulse voltage produced by these cores would cause no harm; however, during the testing of the unit there are times when it is desirable to start the cycle over before it has completed and this will cause the core that was left in the "one" state to return to the "zero" state and the resulting output voltage could spuriously trigger a one shot and the output flip flop. Another reason for this pulse to switch the cores slowly is that this same pulse presets the core flip flop and, if the core of transformer A_0 switches fast, transistor Q_3 will trigger and cause shift line number 2 to be pulsed. This pulse would cause any core sequencer even-numbered core that is in the "one" state to be switched and to produce an unwanted trigger pulse. The output pulse voltage produced when these cores switch over a 20 microsecond interval is far below the pulse voltage amplitude

required to trigger the one shot and flip flop circuit and thus assures that no timing circuit will be triggered at the time the preset pulse is applied.

After the preset line has been pulsed, the next input to the core flip flop causes a current pulse, I_2, to be produced in shift line number 1. This pulse switches core number 1 to the "zero" state and produces a voltage pulse on the 30-turn winding of this core. This voltage pulse produces current pulse, I_1, that flows from the dot side of the 30-turn winding on core number 1 through a diode, the 4-turn primary winding of transformer, T_3, the 50-turn winding on core number 11, the 7-turn winding on core number 2 and back to the non-dot side of the 30-turn winding. Current pulse I_1, produces a voltage pulse on the isolated secondary winding of transformer, T_3, that triggers the output flip flop and a negative-going voltage pulse on the 30-turn winding of core number 2, as core number 2 switches to the "one" state, that triggers the number 1 FET one shot. The voltage pulse from core number 2 is negative with reference to the plus 5 volt supply, which is the d-c voltage applied to the emitter of Q_2 in the FET one shot, which makes it possible to direct couple this point, through a diode, to the base of transistor Q_2. The 50-turn winding on core number 11 is a convenient way of obtaining a small inductance. This inductance is small enough so that it does not affect

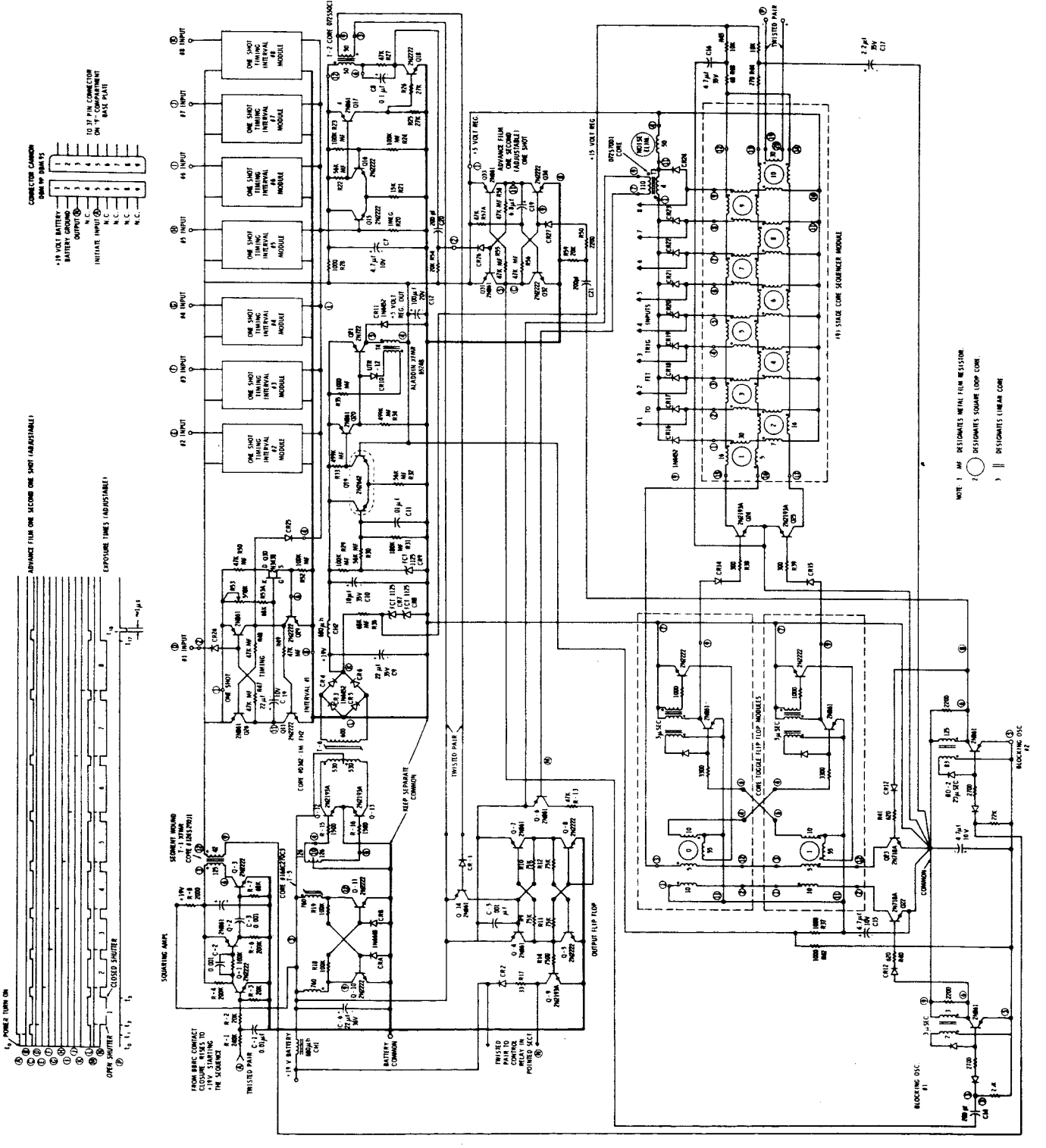
the current pulse that flows when one of the cores switches from a "one" to a "zero" state, but it is large enough to reduce the amplitude of the current pulse that is generated when the "noise" flux switches in the other cores on the shift line. Core number 11 eliminates the noise pulse that appears on the outputs of the cores already in the zero state each time a shift line is pulsed.

The next pulse applied to the input of the core flip flop causes a current pulse, I_3, to appear on shift line number 2. This pulse switches core number 2 to the "zero" state, producing a current pulse, I , which causes a voltage to appear at both output number 2 and the secondary of transformer T_3, which triggers FET one shot number 2 and sets the output flip flop and continues the cycle. This cycle is repeated, as each shift line is alternately pulsed, until core number 10 switches to a "one" state at the end of the last advance-film-timing one shot interval. The current pulse that switches core number 10, produced by core number 9, does not flow through the primary of transformer, T_3, therefore the output flip flop will not be set by this pulse and the cycle will end.

SPECIFICATIONS

A complete timer schematic diagram, including timing waveforms, is shown in Figure 6. Most of the unusual circuits in this schematic have already been discussed, therefore no further comments will be added in the way of explanation of this schematic. A paper explaining the 5 volt regulated supply

Figure 6. Complete Schematic Diagram



is under preparation and will be published at a later time.

The timer has the following electrical specifications:

1. Input Voltage: +16 to +22 volts (nominal 19.5 volts)
2. Input current: 5.4 milliamps maximum at nominal voltage
3. Initiate timing input: 16 volts minimum with a maximum rise time of 10 milliseconds.
4. Maximum load current on output switch: 40 milliamps at nominal power supply voltage
5. Operating temperature range: -50°C. to +60°C
6. Timing interval tolerance: ±5% over the operating temperature range.
7. Timing intervals: 8 intervals
8. Timing period: Each interval independently adjustable from 0.3 seconds to 100 seconds. (This was the range required for this application).
9. Step film period: 1 second ±10%
10. Pulse at end of timing interval: pulse amplitude, 10 volts peak, pulse width 1 microsecond and output impedance 680 ohms. This pulse appears on an isolated line pair

The timer has the following mechanical specifications:

1. Height: 2.8"
2. Width: 2.6"
3. Depth: 3.4"

4. Mounting: flange at bottom of unit with 4 mounting screw holes spaced 3 3/4" x 2 1/16". The mounting flange measures 4 1/4" x 2 3/4".

5. Weight: 376 grams

6. Vibration: 15G, 5 to 2000 cps.